Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
T2147-906625

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____.

Signature _____

Typed or printed name _____

Application Number	Filed
09/706,728	**November 7, 2000**

First Named Inventor
LE QUERE, PATRICK

Art Unit	Examiner
2136	**COLIN**

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☐ attorney or agent of record.
Registration number_____.

☒ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34. **42,736**

Signature

Eric G. King
Typed or printed name

703-610-8647
Telephone number

May 24, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of ____ forms are submitted.

Attorney Docket No. T2147-906625

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

First Named Inventor: LEQUERE, PATRICK

Art Unit: 2136

Application No.: 09/706,728

Examiner: C. G. Colin

Filed: November 7, 2000

Confirmation No.: 8212

For: ARCHITECTURE OF AN ENCRYPTION CIRCUIT IMPLEMENTING VARIOUS TYPES OF ENCRYPTION ALGORITHMS SIMULTANEOUSLY WITHOUT A LOSS OF PERFORMANCE

* * *

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In the outstanding Office Action, Claims 15-18 and 20-34 were rejected under 35 U.S.C. § 103 over Dyke in combination variously with IBM Technical Disclosure Bulletin: Cryptographic Microcode Loading Controller for Secure Function and Bakhle.

However, it is apparent that Dyke does not teach or suggest all of the Claim 15 features for which it is relied upon in the outstanding Office Action. In contrast, Dyke discloses a device having a fundamentally different structure and arrangement.

Independent Claim 15 recites, *inter alia*, an encryption circuit for simultaneously processing various encryption algorithms, the encryption circuit adapted to be coupled with a host computer system comprising: an input/output module, including a microcontroller and memory, that handles data exchanges between the host computer system and the encryption circuit via a dedicated bus, the input/output module further

including a flash memory and a static random access memory, the flash memory storing the code for a processor in the microcontroller, and the processor copying contents of the flash memory into the static random access memory during startup.

With reference to the exemplary embodiment shown in Appellant's disclosure, in particular the figure and page 4 of Appellant's disclosure, the encryption circuit 1 comprises an input/output module 2 that includes a microcontroller 6 and memory (flash memory 7 and static random access memory 8). The encryption circuit 1 further comprises an encryption module 3 and isolation means (dual port RAM 4) that allows the exchange of data and commands/statuses between the input/output module 2 and the encryption module 3. *See* Figure; page 4.

The outstanding Office Action dated January 24, 2007 alleges that Dyke "substantially discloses an encryption circuit (1) for simultaneously processing various encryption algorithms, the encryption circuit adapted to be coupled with a host computer system comprising: an input/output module, including a microcontroller and memory, that handles data exchanges between the host computer system and the encryption circuit via a dedicated bus, for example (see column 3, lines 55-65 and figure 1)." *See* Office Action, page 3, last paragraph, to page 4, line 3.

However, Dyke fails to teach, at minimum, an input/output module including a microcontroller as recited in Claim 15, as illustrated with reference to Dyke's Figure 1 (reproduced below).

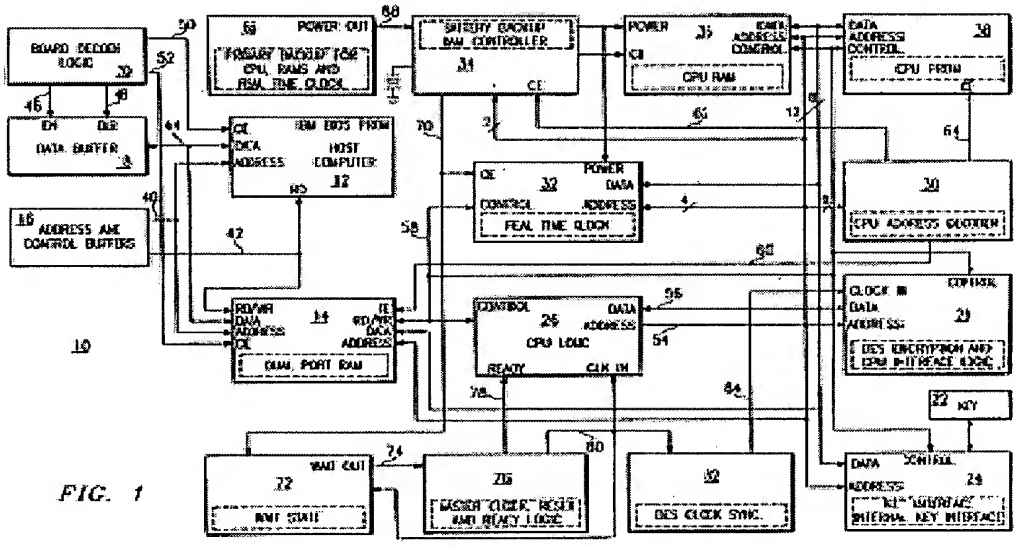

FIG. 1

The portion of Dyke relied upon in the Office Action as allegedly teaching the above-discussed features of Claim 15 provides:

> "The encryption printed circuit board 10 (FIG. 1), hereinafter referred to as the PCB, includes first and second portions. The first portion is an interface between the host computer (for example IBM BIOS PROM) 12 and a first set of ports of a dual port RAM (DPR) 14 and includes in addition to the DPR 14, a plurality of address and control buffers 16, a data buffer 18, and a board decode logic means 20 all having input address ports connected to the host computer. The first portions thus processes the data to be encrypted or decrypted from and to the host processor."

Dyke, col. 3, lines 55-65.

The Office Action apparently relies on Dyke's "host computer (for example IBM BIOS PROM) 12," dual-port RAM 14, address and control buffers 16, and data buffer 18 as allegedly teaching Appellant's input/output module, including a microcontroller and memory, that handles data exchanges between the host computer system and the encryption circuit via a dedicated bus as recited in Claim 15. However, Dyke explains that his "host computer 12" is actually "(for example [an] IBM BIOS PROM) 12" or "host computer PROM 12." See Dyke, col. 3, lines 58-59; col. 5, line 51; *see also* Dyke, FIG. 2b. Dyke thus clearly teaches that his "host computer PROM 12" is merely a

PROM device. Dyke further clearly teaches that his address and control buffers 16 and data buffer 18 are merely buffer devices:

> "Preferably, the host computer PROM 12 may be an IBM or IBM compatible BIOS PROM number 27128 sold by INTEL Corporation, . . . the address and control buffers 16 include a pair of 74 HCT244 buffers sold by Radio Corporation of America, and the data buffer 18 a 74HCT245 sold by Motorola Semiconductor Products, Incorporated."

Dyke, col. 5, lines 60-68; FIG. 2b.

Thus, there is no apparent express teaching or suggestion that Dyke's "host computer PROM 12" or buffers 16 and 18 include a microcontroller and memory, nor would one skilled in the art understand Dyke's Programmable Read Only Memory (PROM) device or buffer devices to inherently disclose a microcontroller, particularly in view of Claim 15's recitation of "a microcontroller" and "memory" as separate structures.

Therefore, it is clear that Dyke does not teach or suggest an input/output module, including a microcontroller and memory, that handles data exchanges between the host computer system and the encryption circuit via a dedicated bus, as recited in Claim 15.

Furthermore, Dyke does not appear to teach or suggest an input/output module that includes a flash memory and a static random access memory. In contrast to the Office Action (see Office Action page 2, lines 21-22), Dyke teaches that his CPU RAM 36 and CPU PROM 38 are components of an "encryption/decryption portion," a second portion that is separate and distinct from Dyke's "interface portion," or first portion, that includes items 12, 14, 16, and 18 alleged by the Office Action to correspond to Appellant's claimed input/output module. Dyke, col. 3, line 66 to col. 4, line 7; Fig. 1.

In addition, regarding Dyke's CPU 26 component, Dyke teaches that CPU 26 is a component of his "encryption/decryption portion" in conjunction with CPU RAM 36 and CPU PROM 38, and therefore CPU 26 cannot correspond to the input/output module of Claim 15. *See* Dyke, col. 4, lines 2-7 and 46-68.

The Office Action does not rely on the secondary references, IBM Technical Disclosure Bulletin: Cryptographic Microcode Loading Controller for Secure Function and Bakhle, to remedy the above discussed deficiencies of Dyke. However, the Advisory Action newly asserts that Dyke's above-discussed deficiencies can be ignored because IBM Technical Disclosure Bulletin allegedly teaches "an input/output module comprising a microcomputer and memory." However, particularly in view of the above-discussed lack of correspondence between Dyke and the features of Claim 15, it is not apparent how the primary reference Dyke could be modified by one skilled in the art to incorporate IBM Technical Disclosure Bulletin's teaching of a single-chip micro-controller to assemble the invention of Claim 15, without requiring the wholesale reconstruction of the primary reference Dyke.

Based on at least the above, Appellant respectfully submits the outstanding rejections are untenable. Appellant respectfully requests withdrawal of the outstanding rejections.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2147-906625) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

May 24, 2007

By: _____
Edward J. Kondracki
Reg. No. 20,604

Eric G. King
Reg. No. 42,736

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

4830-2506-6753